Two-dimensional(2D) subthreshold current and subthreshold swing modeling of double-material-gate(DMG) strained-Si(s-Si) on silicon-germanium(SiGe) MOSFETs

A dissertation submitted in partial fulfilment of

the requirement for the degree of

Masters of Technology in

VLSI Design and Embedded Systems

by

Anand Kumar Mukhopadhyay (212EC2141)

to the

Department of Electronics and Communication Engineering
National Institute of Technology Rourkela

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DEPARTMENT OF ELECTRONICS AND
COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY, ROURKELA
ORISSA, INDIA-769008

CERTIFICATE

This is to certify that the thesis entitled "***Two-dimensional (2D) subthreshold current and subthreshold swing modeling of double-material-gate (DMG) strained-Si (s-Si) on silicon-germanium (SiGe)* MOSFETs**" being submitted by **Anand Kumar Mukhopadhyay** bearing **Roll No. 212EC2141**pursuing **M. Tech.** in the department of Electronics and Communication Engineering in the specialization of **VLSI Design and Embedded Systems** during the session **2012-2014**to the National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance. The research reports and the results discussed in this dissertation have not been submitted in parts or in full to any other University or Institute.

Place: Rourkela

Date: 30th May, 2014

Prof. (Dr.) P. K. TIWARI
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Rourkela – 769008

Dedicated to my parents, teachers and friends

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Anand Kumar Mukhopadhyay

ABSTRACT

In this dissertation analysis of double-material-gate (DMG) strained-Si (s-Si) channel on SiGe substrate MOSFET is done in the subthreshold region of operation and hence the behaviour of leakage current and subthreshold swing is studied. The advantages of dual material gate (DMG) structure to suppress various short channel effects are studied. Also the effect of introducing strain in the channel is incorporated as it is beneficial in terms of improving the mobility of carriers in the channel.

A two dimensional (2D) analytical device model is derived by solving Poisson's equation and by approximating the potential profile as a parabola in the channel. A detailed analysis of double-material-gate (DMG) strained-Si (s-Si) on SiGe MOSFET is done in the subthreshold region of operation in terms of subthreshold current (I_{sub}) and subthreshold swing (S_t) while varying different device parameters such as gate length (L), amount of strain (X), control gate to screen gate length ratio ($L_1 : L_2$), control gate to screen gate metal work function ratio ($\varphi_{M1} : \varphi_{M2}$) to investigate the advantages of incorporating strain and double material gate metal in the proposed device. Thereafter two dimensional (2D) simulation of the device is carried out in the device simulator ATLAS^{TM} by Silvaco Inc. The data extracted from the simulator is used for verification of the predicted model.

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LIST OF SYMBOLS

Gate Oxide Thickness	t_{ox}
Strained Silicon layer Thickness	t_{Si}
Gate Length	$L = L_1 + L_2$
Control Gate Length	L_1
Screen Gate Lengths	L_2
Work function of Control Gate	φ_{M1}
Work functions of Screen Gate	φ_{M2}
Potential profile under Control Gate	$\Psi_1(x,y), \Psi_3(x,y)$
Potential profile under Screen Gate	$\Psi_2(x,y), \Psi_4(x,y)$
Surface Potential	$\varphi_{si}(x)$
Source and Drain Doping	N_d
Channel Doping	N_a
Mobility	μ_n
Gate to Source Voltage	V_{GS}
Drain to Source Voltage	V_{DS}
Threshold Voltage	V_t
Subthreshold Current	I_{sub}
Subthreshold Swing	S_t

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CHAPTER 1

INTRODUCTION

1.1.Semiconductor: A Brief History

In the early 1830s a renowned scientist Michael Faraday observed that resistance of silver sulfide decreases with rise in temperature which was unlike of that observed in metals. At the end of the decade around 1839 another great scientist revealed photovoltaic effect. Both the scientists exploited the intrinsic properties of semiconductor. In the early 1870s, Karl Braun invented point contact diodes which could replace the vacuum tube diode. Later Braun along with Marconi got noble prize for their invention in 1909. During 1873, scientist W. Smith observed photoconductivity in selenium. Further in 1876 photovoltaic effect was discovered for the first time by Adams and Day. In 1878 Hall Effect was discovered by the famous scientist E.H. Hall and in 1880s, magnetoresistance was studied in solid state by J.J.Thompson. In 1900, scientist Plank introduced the concept of quantum mechanics whereas Einstein discovered photoelectric effect. The word semiconductor was coined in 1910. In 1920 inventor Lilienfield proposed semiconductor triode to replace vacuum tube triode. The theory of rectifying junctions and energy band model was established in the 1930s. Further in the 1950s the invention of first solid state amplifier took place which is the Bipolar Junction Transistor. Thereafter Noyce and Kilby introduced the planar process used in integrated circuits for which Kilby got the noble prize for his invention of integrated circuits [1].

Thereafter, a series of solid state devices have been proposed. Introduction of MESFETs, OPAMPs and Small Scale Integration (SSI) took place in the 1960s. Then integration of devices into ICs started in the form of Medium Scale Integration (MSI) in which filters, 256 bit RAM and Registers were made. Then Large Scale Integration (LSI) was made possible in which up to 16K RAM, A/D converters, microprocessors were made. Thereafter in in 1980, High Electron Mobility Transistor (HEMT) was discovered which falls under Very Large Scale Integration (VLSI) which made possible 64Kbit RAM memories and computers. Further in 1990s, 3-D integration took place in which semiconductors could not only be integrated in a plane but also in vertical dimension. Then in 21st century the field of nanoelectronics started emerging wherein nano dimension devices were made of nano crystalline materials. The reduction in size of the transistors which is termed as scaling has gone to a great extent but has limitations as various problems arise due to further scaling in the nanoscale level.

1.2.Scaling

As per Moore's law which states that "The numbers of transistors incorporated in a chip will approximately double every 24 months" which has been true till date due to shrinking of the transistor size with time which is termed as scaling [2]. As MOSFET is an important transistor to study in the 20th century due to its immense use in different CMOS circuits which consume less power with a faster speed of operation, it is important to study the ways of scaling that can be implemented in MOSFETs. Basically there are three types of scaling methods which are [3]:

(a) Constant Field Scaling

(b) Constant Voltage Scaling

(c) General Scaling

In constant field scaling, the electric fields in the horizontal and vertical directions are kept constant. The parameters such as device channel length, channel width, gate oxide thickness, gate oxide capacitance, junction depth, power supply voltage, threshold voltage are scaled down by the scaling factor k. In this case the doping level should be scaled up by a factor k. The drain current in linear and saturation mode of operation are also scaled down by factor k. As power dissipated by the device is the product of drain current and drain to source voltage, it is reduced by a factor k^2 after scaling which is an advantage of constant field scaling. But the power density which is the power dissipated per unit area remains unchanged even after scaling. The problem associated in constant field scaling is that the designers need to scale down the external voltage level which is a constraint. Also as the threshold voltage of the device is scaled down there is a significant increase in leakage current which increase the static power dissipation when the device is in the subthreshold region of operation.

In constant voltage scaling all the device dimensions are allowed to be scaled except voltages. The parameters such as channel length, channel width, gate oxide thickness, junction depth are scaled down by a factor k while the power supply external voltage and threshold voltage remain unchanged after scaling. Therefore the doping densities are increased by a factor k^2. The gate oxide capacitance gets increased by a factor k which implies that the drain current in the linear mode and saturation mode of operation gets increased by a factor k. Hence the power dissipated by the device is increased by a factor k and the power density by a factor k^3. Though it has advantages over constant field scaling in terms of fixed external voltage levels, the disadvantage is the large increase in the current and power densities which cause problems such as oxide-breakdown, hot-carrier degradation, electromigration and electrical overstress which are serious reliability problems.

In general scaling there is usually a larger increase in doping and smaller decrease in supply voltage. In this case the scaling factor is not kept fixed. Suppose s is the scaling factor then 1<s<k will be the range of the scaling factor. The parameters such as channel length, channel width, gate oxide thickness, junction depth are scaled by a factor k. The doping level is scaled up by a factor k and the supply voltage is scaled by a factor s/k. To achieve a tradeoff between constant field scaling and constant voltage scaling general scaling is implemented.

1.2.1. Challenges in Scaling

But as the transistor feature size is reduced to the nanometer level various problem arise which are known as short channel effects. The SCE's caused due to vertical scaling are polysilicon depletion effect, quantum effects and gate tunneling whereas SCEs caused due to lateral scaling are threshold voltage roll-off, DIBL, hot carrier effect and mobility degradation.

1.2.2. Methods to Overcome Challenges in Scaling

The overcome the problems various methods have been introduced in the form of gate and channel engineering techniques. Using high-k dielectric, metal gate and multiple gates are some of the prominent means of gate engineering techniques whereas use of shallow S/D junction, halo doping, strain and multi-material gate are the efficient means to introduce channel engineering techniques.

1.3.Motivation

From the various engineering techniques applied in the channel and gate of MOSFET, strain in the channel and double-material-gate (DMG) have been chosen in the proposed device. The prominent features of strain is to increase the mobility of carriers in the applied region, in this case channel whereas the advantage of double-material-gate (DMG) is in reducing short channel

effects (SCEs) by creating a shield to the minimum channel potential profile from the drain voltage applied and hence providing immunity to SCEs like drain induced barrier lowering (DIBL) and hot carrier effects (HCEs). The following techniques are explained below:

1.3.1. Double-material-gate (DMG)

Using multi-material gate is an efficient mean to minimize short channel effects such as hot carrier effects (HCEs) and drain-induced-barrier-lowering (DIBL). In this case DMG structure is used in which two different metals are used as shown in fig.1.1.

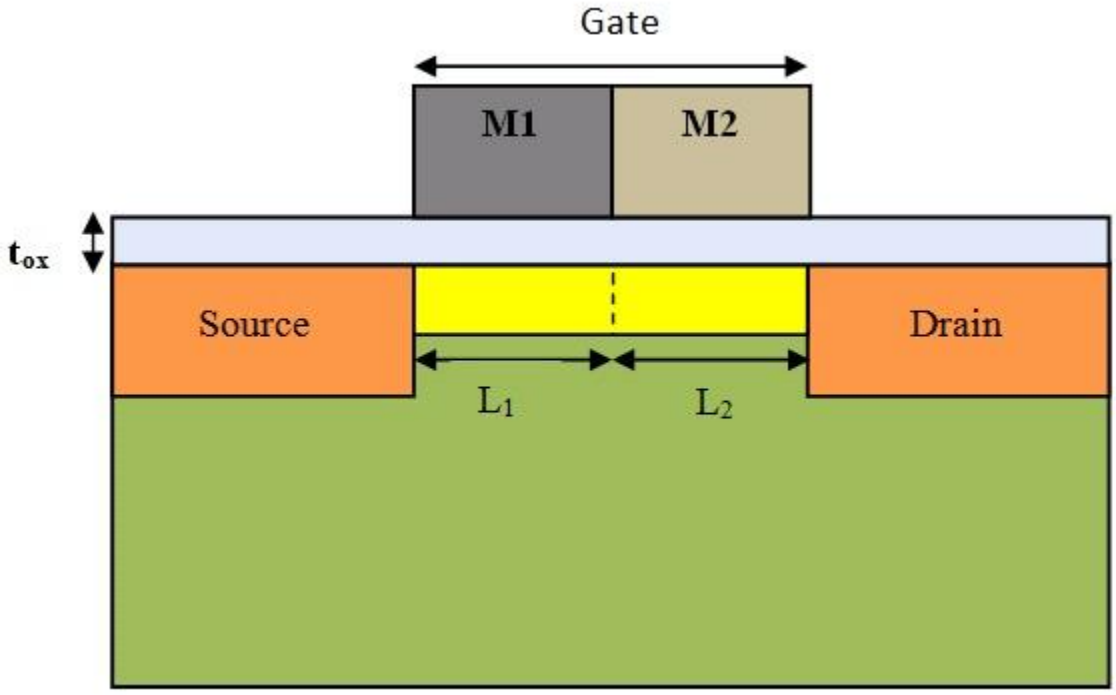

Fig.1.1 Schematic of double-material-gate (DMG) structure.

Here M1and M2 are known as the control gate and screen gate respectively in which M1 has a greater work function than M2. This affects the potential profile in the channel. The two

regions formed under the channel are divided into L_1 and L_2 where $L = L_1 + L_2$ is the total length of the channel.

1.3.2. Strain

In our proposed structure the doping level in the channel is fixed at a high level in the order of $10^{18}_{cm}{}^{-3}$. But due to higher doping, impurity scattering takes place which have a serious effect in degrading the mobility of the carriers. So a very promising technology is incorporated to improve the mobility of carriers in the channel region which is strain technology. The material taken in the substrate is SiGe and in the channel is Si. Here biaxial strain is created due to the difference in lattice constant of Si and Ge in which Si has a smaller lattice constant as compared to Ge. A schematic diagram is shown in fig.1.2 in which the blue colored atoms are of smaller lattice constant (in this case Si) and the red colored atoms are of larger lattice constant (in this case SiGe). After the epitaxial growth of Si on SiGe biaxial strain is generated. The amount of strain can be increased or decreased by varying the concentration of Ge in the substrate as it is directly proportional to the amount of strain induced in the channel. Due the strain the electron mobility in the channel can be enhanced up to 2.3 times when the amount of Ge concentration in the $Si_{1-X}Ge_X$ substrate is about 30% [4].

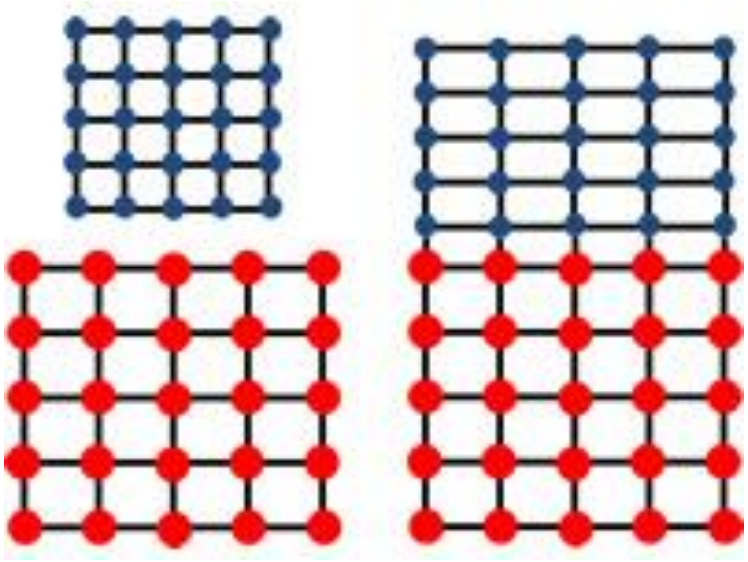

Fig.1.2 General diagram to generate biaxial strain.

1.4.Thesis Organization

Chapter 1: This chapter presents a brief history of semiconductor. Also the problems associated to scaling and the methods to overcome it are discussed.

Chapter 2: In this chapter the literature review is done for different strained MOSFETs. Further the proposed device structure which is DMG s-Si on SiGe substrate MOSFET is discussed along with the problem statement of the dissertation.

Chapter 3: This chapter presents a brief description to use ATLAS device simulator to simulate any device.

Chapter 4: This chapter presents the analytical model of subthreshold current of DMG s-Si on SiGe substrate MOSFET which has been verified through simulation results.

Chapter 5: This chapter presents the analytical model of subthreshold swing of DMG s-Si on SiGe substrate MOSFET which has been verified through simulation results.

Chapter 6: This chapter discusses the outcome of the thesis and the scope for future work.

CHAPTER 2

LITERATURE REVIEW

2.1. Fabrication

In the year 2000, K. Rim et. al. [5] fabricated a deep submicron strained-Si n-MOSFET. It was fabricated on strained Si/relaxed $Si_{0.8}Ge_{0.2}$ heterostructures. A comparative study of strained and unstrained Si surface channel device was done. It is observed that the mobility of the strained-Si device is improved by about 75% even when the substrate is heavily doped with high vertical fields. The intrinsic transconductance of the strained Si devices is almost increased by 60% for channel lengths ranging from 1 to 0.1μm. The performance improvement in strained Si is due to the increase in low-field mobility and improved high-field transport which is due to the reduction in carrier-phonon scattering for electrons. These improvements in strained-Si n MOSFET's are due to the strain-induced energy splitting that aids in reduction of the density of final states and hence reduces the phonon-assisted scattering rate for electrons with average energies in the maximum range of few hundred meV.

In 1999, Xiang et al. [6] filed a patent explaining the technique to fabricate dual-metal-gate (DMG) MOSFET. This invention comprises a new technique to realize a dual-material-gate (DMG) MOSFET. The inventive technique is based upon an asymmetric oxide spacer formation and a self-aligned silicide formation. The asymmetric oxide spacer on the sidewall of the drain side of the gate is formed by selectively etching the spacer on the source side. The etch selectivity is realized by nitrogen implantation into an oxide spacer on the source side, by

utilizing preferably an angled ion implantation technique. An HF solution has been experimentally demonstrated to provide an etch rate of the nitrogen implanted oxide that is much faster than the oxide without the nitrogen implantation.

In 2006, P.F. Hsu et. al. [7] reported an advanced method to fabricate a dual metal gate MOSFET using high-k dielectric which uses TaC for nFETs and MoN_x for pFETs to achieve low threshold voltage. Non uniformity in V_t is induced due to high –k crystallization in small devices. Enhanced carrier mobility, excellent threshold voltage control and compatibility with strained-Si module are observed which is favourable for various CMOS applications.

2.2. Early Work

In 1954, C.S. Smith [8] observed the piezoresistance effect in Germanium and Silicon in which he found that uniaxial tension is created which is the main cause for the change of resistivity in both n and p type silicon and germanium.

In 1999, Long et.al. [9] showed the advantages of dual-material-gate(DMG) FET which is possible due to the material work function difference in the control and screen gate which makes the threshold voltage near the source greater than that near the drain in case of n-channel FET, which results in a rapid acceleration of charge carriers in the channel and also provides screening effect to overpower short-channel effects.

In 2005, M.L. Lee et. al. [10] did a focussed review on strained Si, SiGe and Ge channels for high mobility MOSFETs in which an extensive research was done from the year 1980 to the 21st century on various discoveries made in the field.

In 2006, M. Jagadesh Kumar et. al. [11] developed a simple and accurate analytical model for the threshold voltage of nanoscale single-layer fully depleted strained-silicon-on-insulator MOSFETs by solving 2D Poisson's equation in which several important parameters such as the effect of strain, short-channel effects, strained-silicon thin film doping, strained-silicon thin-film thickness, gate work function and other device parameters were discussed. It is seen that there is a decrease in threshold voltage with increasing strain in the silicon thin film.

In 2007, Jagadesh Kumar et. al. [12] developed a compact analytical model which discusses the impact of strain on the threshold voltage of nanoscale strained-Si/SiGe MOSFETs. Strain or Ge content on the threshold voltage of nanoscale strained-Si/SiGe bulk MOSFETs was made. The effects of strain (Ge mole fraction in SiGe substrate), short-channel length, source/drain junction depths, substrate (body) doping, strained silicon thin-film thickness, gate work function and other device parameters were analysed. A decrease in threshold voltage with increasing strain was also observed.

In 2010, Li Jin et. al. [13] developed a two-dimensional threshold voltage analytical model of DMG strained-silicon-on-insulator MOSFETs. They investigated the improved short channel effect (SCE), hot carrier effect (HCE), drain-induced barrier-lowering (DIBL) and carrier transport efficiency for their proposed device.

In 2011, Li Jin et. al. [14] developed a new accurate 2D analytical model comprising surface channel potentials, a surface channel electric field and threshold voltage for fully depleted asymmetrical dual material gate double-gate strained-Si MOSFETs.

In 2012, Shiv Bhusan et. al. [15] developed an analytical model for the threshold voltage of short-channel double-material-gate (DMG) MOSFETS with a strained-silicon (s-si) channel on silicon-germanium (SiGe) substrates.

2.3. Device Structure

The schematic diagram of the proposed device which is double-material-gate (DMG) strained-silicon(s-Si) on $Si_{1-X}Ge_X$ substrate is shown in Fig.2.1 and Fig.2.2 showing the cross sectional view and with the BOX approximation of depletion region [15] respectively. In fig.2.1, x_{dl}, x_{dv} and N_a are the lateral source/drain depletion width, vertical depletion width and substrate doping respectively.

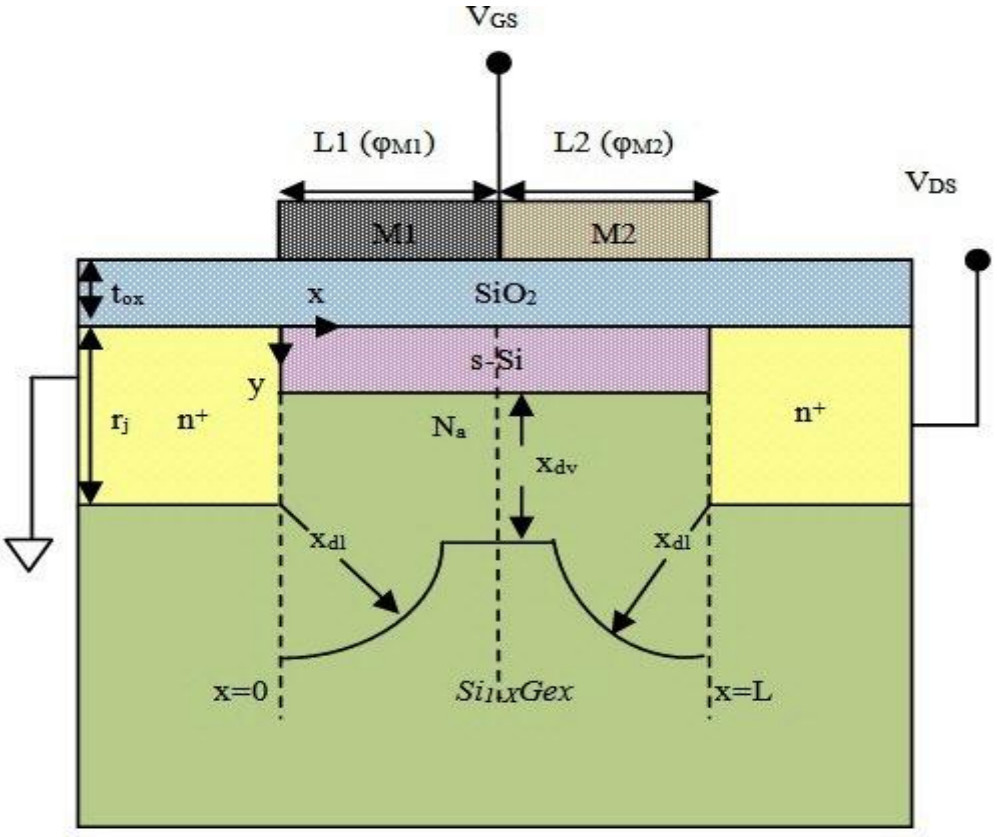

Fig.2.1 The structure of DMG $s-Si$ on $Si_{1-X}Ge_X$ MOSFET used in simulation [15].

In Fig.2.2, t_{ox}, t_{Si}, r_j, L and $N_{a,eff}$ are the gate oxide thickness, strained-silicon channel thickness, source/drain height, channel length and effective doping as approximated in the depletion box respectively. The gate electrode is formed using two different metals (M_1 and M_2) with work functions φ_{M1} and φ_{M2} respectively having the respective gate lengths L_1 and L_2 where $\varphi_{M1} > \varphi_{M2}$ and $L = L_1 + L_2$. The metal gate near the source terminal is of higher work function (φ_{M1}) and is known as the control gate whereas the metal gate near the drain terminal is chosen to be of lesser work function (φ_{M2}) relative to the control gate which is known as the screen gate due to its ability to screen the minimum potential point from varying voltage fluctuations at the drain side.

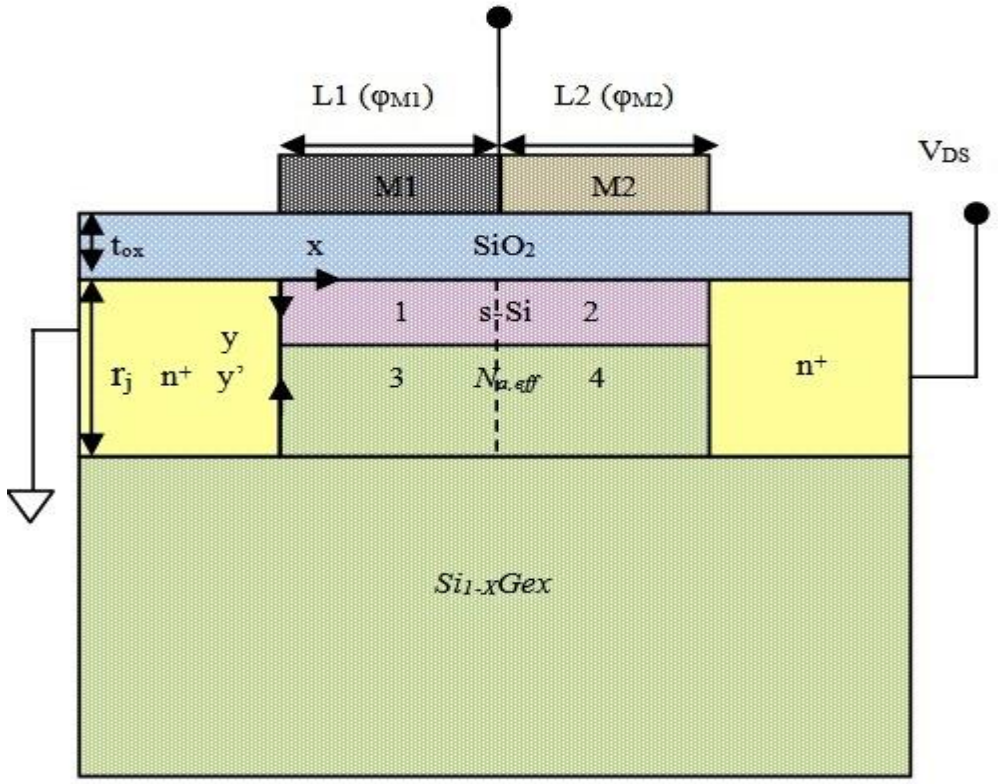

Fig.2.2The structure of DMG $s-Si$ on $Si_{1-X}Ge_X$ MOSFET (with BOX approximation of depletion region) [15].

The depletion approximation made in the channel region is done to determine the effective doping in the box which has been used by M. J. Kumar et al. [12] which is mentioned below:

$$N_{a,eff} = N_a\left[1-\left(\left(1+\frac{2x_{dv}}{r_j}\right)^{1/2}-1\right)\times\frac{r_j}{L}\right] \quad (1)$$

where,

$$x_{dv} = \sqrt{\frac{2\varepsilon_{SiGe}(\phi_{th}-V_{sub})}{qN_a}} \quad (2)$$

$$\phi_{th} = 2\phi_{f,Si} + \Delta\phi_{(s-Si)} \quad (3)$$

Here, ϕ_{th} is the minimum value of surface potential required for inversion to take place.

2.4. Research Problem Statement

The study on important characteristics such as subthreshold current and subthreshold swing is done on double-material-gate (DMG) strained-silicon (s-Si) on silicon-germanium (SiGe) MOSFET with the help of 2-D analytical model and numerical data collected using the device simulator ATLAS by Silvaco Inc.

CHAPTER 3

ATLAS DEVICE SIMULATOR

3.1 Introduction

ATLAS is software by Silvaco which has capabilities for physically based two dimensional and three dimensional simulations of semiconductor devices. The prime feature of ATLAS includes the comprehensive set of models, compatibility with other software by Silvaco and powerful numerical techniques [16]. The Virtual Wafer Fab (VWF) INTERACTIVE TOOLS such as DECKBULID, TONYPLOT, DEVEDIT, MASKVIEWS and OPTIMIZER which provide an interactive runtime environment are often used in combination with ATLAS.

ATLAS can predict the electrical characteristics which are associated with the physical structure of the device and the bias conditions applied hence also known as a physically based device simulator. This can be achieved by approximating the device into 2D or 3D grid in which the intersecting grid points are called nodes. The mesh size is altered in different portions of the device as per requirement. For instance fine mesh is assigned at the junction of source and channel in case of a MOSFET. The transport of carriers is simulated by solving set of differential equations which are derived from Maxwell's laws, i.e. , the electrical performance of the device can be determined in various modes of operation such as DC, AC or transient. To specify the problem to be simulated the following are defined [16]:

a. The physical structure of the device.

b. The physical models used.

c. The biasing conditions applied.

3.2 Program Flow

The sequence in which the program is written in the deckbuild file must be followed for the execution of the program. The program is basically divided into five groups as shown below:

Group	*Statements*
1. Structure Specification	MESH REGION ELECTRODE DOPING
2. Material Models Specification	MATERIAL MODELS CONTACT INTERFACE
3. Numerical Method Selection	METHOD
4. Solution Specification	LOG SOLVE LOAD SAVE
5. Results Analysis	EXTRACT TONYPLOT

The statements in each group should also be written in correct order for successful running of the program otherwise the program will run incorrectly or get terminated.

3.3 Syntax

In the following section syntax for various parts of the program are discussed. Firstly, we define the structure using the command language as follows:

3.3.1 Mesh Specification

The first statement that is written is

MESH SPACE.MULT=<VALUE>

Then using x and y coordinate systems the structure meshing is doneas follows:

X.MESH LOC=<VALUE> SPAC=<VALUE>

.

.

.

Y.MESH LOC=<VALUE> SPAC=<VALUE>

.

.

.

The mesh size can be finer or coarser by scaling it up or down using the first statement. For example SPACE.MULT=1 will create finer mesh which will increase the accuracy whereas SPACE.MULT=8 will create coarser mesh reducing the accuracy but increasing the speed of the simulation. The location values are specified in microns.

3.3.2 Region and Material Specification

Next the materials used in the structure are divided into regions and are given serial numbers starting from 1. For example to define the channel of 90nm length and thickness 10nm the statement can be written as:

REGION NUMBER=4 X.MIN=0.00 X.MAX=0.090 Y.MIN=0.00 Y.MAX=0.010 MATERIAL=SILICON

Here the material used in the channel is silicon and the region number is set to 4.

3.3.3 Electrode Specification

Here the electrodes are defined which are required in the structure. A maximum of 50 electrodes can be defined. For example to define the electrode at the drain side of a MOSFET the following statement can be written:

ELECTRODE NAME=DRAIN NUMBER=1 X.MIN=0.120 X.MAX=0.120 Y.MIN=0.0 Y.MAX=0.045

3.3.4 Doping Specification

Next the doping in the different regions defined earlier is specified. Doping can be uniform as well as Gaussian. Examples for both are as follows:

DOPING UNIFORM CONC=1E18 N.TYPE DIRECTION=Y REGIONS=5

DOPING GAUSSIAN CONC=2E18CHARACTERISTIC=0.05 N.TYPE X.LEFT=0.0 X.RIGHT=1.0 PEAK=0.1

In the first statement n type uniform doping with a concentration of 1e18cm^{-3} is done in region 5. In the second statement n type Gaussian doping is done with the peak concentration fixed to 2e18 cm^{-3} along the range x=0 to x=1µm.

3.3.5 Material and Model Specification

The material parameters such as band gap, density of states, permittivity, mobility and affinity can be specified by the user for different regions. If not specified then the default values will be considered. To set the band gap of material in region=4 to 0.96eV the following is written:

MATERIAL REGION =4 EG300=0.96

The model section is used to define the models which are to be considered for a specific structure. The physical models used are broadly classified into the following categories:

a) Carrier Statistics models

b) Mobility models

c) Recombination models

d) Impact Ionization models

e) Tunnelling models and Carrier Injection models

Based on the requirement a compatible combination of the models is specified.

3.3.6 Contact and Interface Specification

The electrodes which are in contact to the device structure are supposed to be an ohmic contact by default. The work function of the metal electrode can be mentioned in the code as follows:

CONTACT NAME=FGATE WORKFUNCTION=4.71

In the above statement the work function of metal gate is set to 4.71 eV which forms a Schottky contact. When external voltage supplied used is same for different metal electrode contacts then the following statement is used to link them

CONTACT NAME=FGATE2 WORKFUNCTION=4.4 COMMON=FGATE

Here FGATE2 is the metal electrode of screen gate with a work function of 4.4 eV which is linked to FGATE which is the metal electrode of control gate with a work function of 4.71 eV as the gate voltage to be supplied is common for both.

For defining the interface trap charges between an interface between a semiconductor and insulator the following statement is written:

INTERFACE QF=3e10 X.MIN=1.0 X.MAX=2 Y.MIN=0.0 Y.MAX=0.5

Here a charge of 3e10 cm^{-3} is defined in the rectangular region specified by X.MIN, X.MAX, Y.MIN, Y.MAX coordinates.

3.3.7 Method Specification

The numerical methods which can be used to solve the Poisson's equation of the device are defined in the methods section. Basically, ATLAS provides three different types of techniques to

solve which are (a) GUMMEL (decoupled), (b) NEWTON (fully coupled) and (c) BLOCK. For weakly coupled system of equations having linear convergence GUMMEL method is used which also has the ability to provide a better initial guess. For strongly coupled system of equations with quadratic convergence NEWTON method is used. However for solving constant quantities which are weakly coupled NEWTON method may take more time to solve. An accurate initial guess is needed in the case of NEWTON method to obtain convergence. In these cases, BLOCK method provides simulation at greater speeds when compared to NEWTON.

3.3.8 Solution Specification

The solutions such as DC, AC, transient and small signal are possible to solve in ATLAS. Firstly, the statement SOLVE INIT is written which sets the initial solution at thermal equilibrium. To define a DC bias which sets the gate voltage to 1V the following statement is written:

```
SOLVE VGATE=1
```

Next the LOG files are defined which store the terminal characteristics of the device in terms of voltage and current. For example the statement defined below creates a file with name PROG1.

```
LOG OUTF=PROG1.LOG
```

Next for varying the DC voltage of an electrode the following statement is written:

```
SOLVE VDRAIN=0.0 VSTEP=0.01 VFINAL=.05 NAME=DRAIN
```

Here the drain voltage is varied from 0 V to 0.05 V with a step size of 0.01 V. To vary an AC bias of frequency 1 GHz at the gate terminal the following statement is written:

```
SOLVE VGATE=0.0 VSTEP=0.05 VFINAL=1.0 NAME=GATE AC FREQ=1.0e9
```

Next the SAVE statement is used which is used to generate structure file as shown:

```
SAVE OUTF=PROG1.STR
```

3.3.9 Result Analysis

Finally we can use extract command to get the values of certain device parameters such as threshold voltage and subthreshold swing. For example to extract threshold voltage of the device the following code is written:

```
EXTRACT NAME="Vt" XINTERCEPT (MAXSLOPE (CURVE (V."GATE",(I."DRAIN"))) -
(AVE(V."DRAIN"))/2.0)
```

Also to get the structure and current characteristics in graphical form tonyplot is used.

```
TONYPLOT PROG1.STR

TONYPLOT PROG1.LOG
```

In the above statements the structure file and log file are accessed by tonyplot and the graphical representation is obtained.

Table 3.1Important device parameters used in simulations.

Parameters	**Value**
Mole Fraction(X)	0-30%
Source /Drain doping (N_d)	$2e20\text{cm}^{-3}$
Channel doping (N_a)	$1e18\text{cm}^{-3}$
Oxide thickness (t_{ox})	2 nm
Source/Drain height(r_j)	45 nm
Channel Length (L)	70,90,110nm
Strained-Silicon film thickness (t_{si})	10 nm
Control Gate Metal work-function (M_1)	4.6,4.71,4.8,4.9 eV
Screen Gate Metal work-function (M_2)	4.4 eV

Table 3.2 Modified parameter values of silicon after the application of strain (X)

Parameter	*X=0.0*	*X=0.1*	*X=0.2*	*X=0.3*
E_g300(eV)	1.08	1.04	1.00	0.96
N_c300 (cm^{-3})	2.80e19	2.25e19	1.98e19	1.95e19
N_V300(cm^{-3})	1.04e19	7.80 e18	5.85e18	4.39e18
Permittivity	11.8	11.8	11.8	11.8
Mobility (cm^2/V.s)	1400	1800	2250	2305
Affinity (eV)	4.17	4.23	4.28	4.34

CHAPTER 4

SUBTHRESHOLD CURRENTFORMULATION

4.1. Modeling of Parameters

In the mentioned device strain is created due to the fact that there is a mismatch in lattice constant of Si (5.431Å) and Ge (5.657Å). The strain created is biaxial in nature as silicon is grown over $Si_{1-X}Ge_{1-X}$ layer. The amount of strain increases with the increase in the concentration of Ge mole fraction (denoted by X) in the $Si_{1-X}Ge_{1-X}$ substrate which corresponds to improvement in the mobility of carriers in the channel. The modified band structure is shown in Fig.4.1 which shows the effect of strain on the energy levels of strained Si and relaxed $Si_{1-X}Ge_{1-X}$ layer which can be modelled as [13]

$$(\Delta E_c)_{s-Si} = 0.57X \tag{4}$$

$$(\Delta E_g)_{s-Si} = 0.4X \tag{5}$$

$$V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \approx 0.075X \tag{6}$$

$$\varepsilon_{SiGe} = 11.8 + 4.2X \tag{7}$$

The above equations are the affected parameters due to strain which are the change in conduction band energy level $((\Delta E_c)_{s-Si})$, change in energy band gap for silicon $((\Delta E_g)_{s-Si})$ and

permittivity of $Si_{1-X}Ge_{X}(\varepsilon_{SiGe})$ respectively. The density of states in the valance band of unstrained-Si and strained-Si are represented as $N_{V,Si}$ and $N_{V,s-Si}$ respectively.

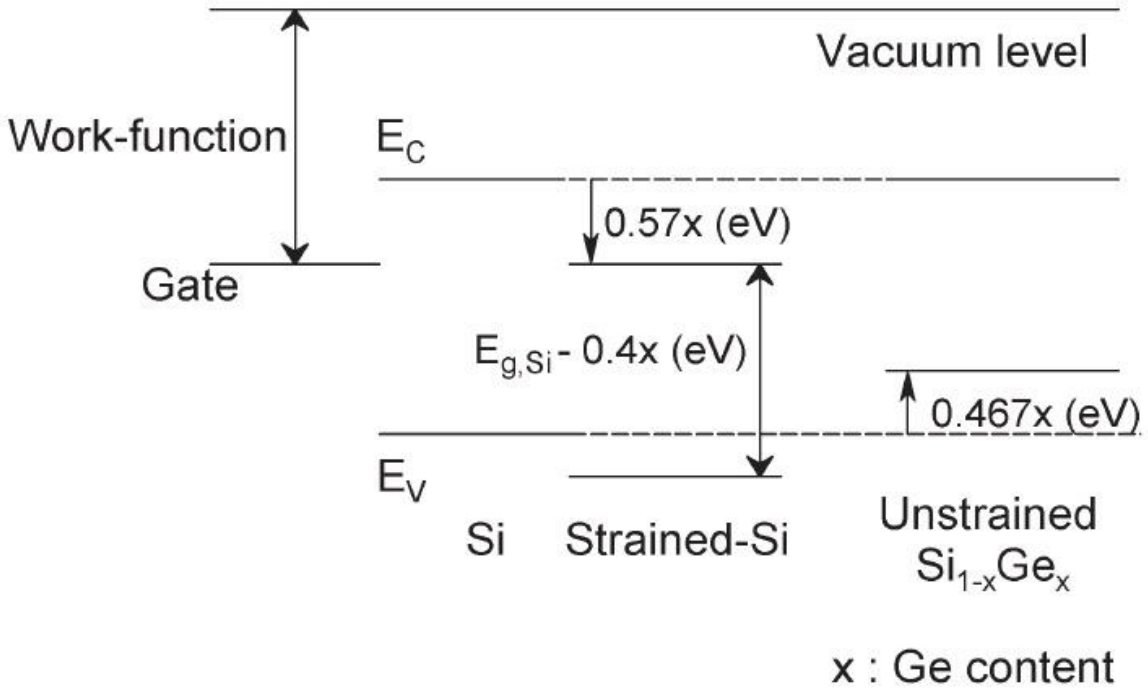

Fig.4.1 Energy band diagram alteration due to strain [17].

This results in the deviation of vital parameters such as the flat band voltage and built in potential which is represented as follows:

$$(V_{FB,f})_{sSi} = (V_{FB,f})_{Si} + \Delta V_{FB,f} \tag{8}$$

$$\text{Where, } \Delta V_{FB,f} = \frac{\{-(\Delta E_c)_{s-Si} + (\Delta E_g)_{s-Si}\}}{q} - V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right) \tag{9}$$

$$V_{bi,sSi} = V_{bi,Si} + (\Delta V_{bi})_{s-Si} \tag{10}$$

where, $\Delta V_{bi,sSi} = -\frac{\left(\Delta E_g\right)_{s-Si}}{q} + V_T \ln\left(\frac{N_{V,Si}}{N_{V,s-Si}}\right)$ (11)

Here, $\left(V_{FB,f}\right)_{sSi}$ and $V_{bi,sSi}$ are the flat band voltage and built in potential of strained Si in which $\left(V_{FB,f}\right)_{Si}$ and $V_{bi,Si}$ are the flat band voltage and built in potential of unstrained silicon in which $\Delta V_{FB,f}$ and $\left(\Delta V_{bi}\right)_{s-Si}$ are the change in flat band voltage and built in voltage due to strain created in the channel.

The 2-D Poisson's equation is solved along with the boundary conditions to obtain the two dimensional potential in the channel which are written as follows:

$$\frac{\partial^2 \Psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x,y)}{\partial y^2} = \frac{qN_{a,eff}}{\varepsilon_{Si}} \quad (12)$$

$$\frac{\partial^2 \Psi_i(x,y)}{\partial x^2} + \frac{\partial^2 \Psi_i(x,y)}{\partial y^2} = \frac{qN_{a,eff}}{\varepsilon_{SiGe}} \quad (13)$$

Here, q, ε_{Si}, ε_{SiGe} and $N_{a,eff}$ [15] are electronic charge, silicon permittivity, silicon-germanium permittivity and effective channel doping, respectively. The simulated structure of DMG s-Si on SiGe MOSFET for the case with L=90nm is shown in Fig.4.2 in which Ge mole fraction content is taken to be 30%. The s-Si region is given in yellow colour whereas the relaxed SiGe is given in green colour below the gate metal. The 2D potential is expressed using parabolic approximation in the regions 1,2,3,4 as shown in Fig. 2.2 in which 1 and 2 are the strained regions under control gate and screen gate respectively whereas 3 and 4 are relaxed $Si_{1-X}Ge_X$ region under the control gate and screen gate respectively.

$$\Psi_i(x,y) = \varphi_{si}(x) + C_{i1}(x)y + C_{i2}(x)y^2 \tag{14}$$

$$\Psi_i(x,y') = V_{sub} + C_{i1}(x)y' + C_{i2}(x)y'^2 \tag{15}$$

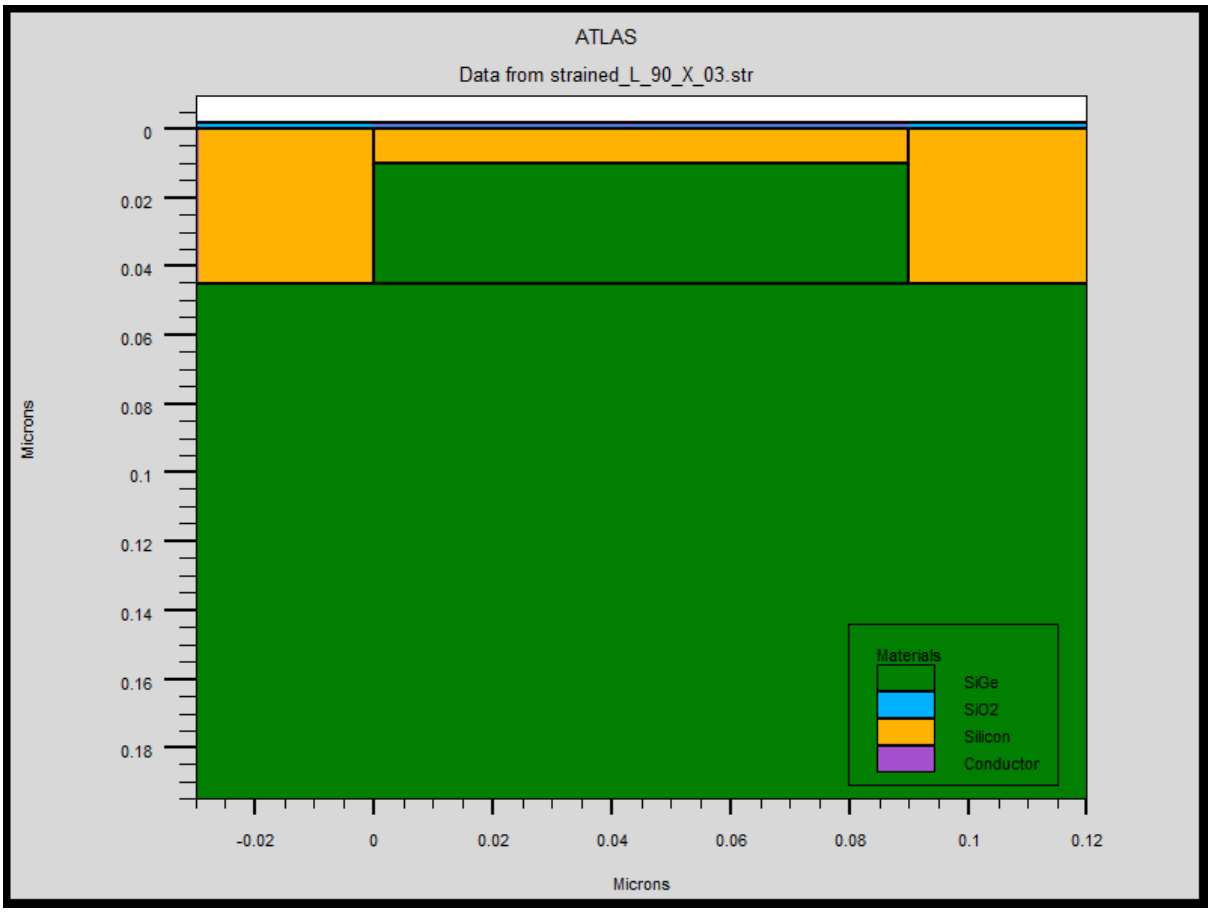

Fig.4.2 Structure of DMG s-Si on SiGe MOSFET extracted from tonyplot with L=90nm.

In the above equation (14) and (15), $\varphi_{si}(x)$ is the surface potential at gate oxide (SiO_2) and channel(s-Si) interface whereas V_{sub} is the voltage applied at the substrate respectively. The boundary conditions involved are mentioned below:

1) The potential and electric field across the interface of the two metals in the channel are continuous.

$$\Psi_1(L_1,0) = \Psi_2(L_1,0) \tag{16}$$

$$\Psi_3(L_1,0) = \Psi_4(L_1,0) \tag{17}$$

$$\left[\frac{\partial\Psi_1(x,y)}{\partial x}\right]_{x=L_1} = \left[\frac{\partial\Psi_2(x,y)}{\partial x}\right]_{x=L_1} \tag{18}$$

$$\left[\frac{\partial\Psi_3(x,y')}{\partial x}\right]_{x=L_1} = \left[\frac{\partial\Psi_4(x,y')}{\partial x}\right]_{x=L_1} \tag{19}$$

2) Continuity of electric flux at the gate oxide and channel interface for both regions 1 and 2 respectively are:

$$\left[\frac{\partial\Psi_1(x,y)}{\partial y}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_{s1}(x)-V_{g1}}{t_{ox}} \tag{20}$$

$$\left[\frac{\partial\Psi_2(x,y)}{\partial y}\right]_{y=0} = \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{\varphi_{s2}(x)-V_{g2}}{t_{ox}} \tag{21}$$

where ε_{ox} and t_{ox} are the dielectric constant and thickness of the gate oxide SiO_2. ε_{Si} is the permittivity of strained-Si. Here,

$$V_{g1} = V_{GS} - (V_{FB1,f})_{s-Si} \tag{22}$$

$$V_{g2} = V_{GS} - (V_{FB2,f})_{s-Si} \tag{23}$$

where V_{GS} is the applied gate to source voltage and V_{g1} and V_{g2} are the effective gate voltage at the gate oxide and channel interface respectively.

3) Electric field at the bottom edge of the depletion region consisting of relaxed $Si_{1-X}Ge_X$ in regions 3 and 4 is zero

$$\left[\frac{\partial \Psi_3(x,y')}{\partial y'}\right]_{y'=0} = 0 \tag{24}$$

$$\left[\frac{\partial \Psi_4(x,y')}{\partial y'}\right]_{y'=0} = 0 \tag{25}$$

4) Continuity of potential and electric field at the strained-Si and $Si_{1-X}Ge_X$ interface

$$\Psi_1(x, t_{Si}) = \Psi_3(x, t_{SiGe}) \tag{26}$$

$$\left[\frac{\partial \Psi_1(x,y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial \Psi_3(x,y')}{\partial y'}\right]_{y'=t_{SiGe}} \tag{27}$$

$$\Psi_2(x, t_{Si}) = \Psi_4(x, t_{SiGe}) \tag{28}$$

$$\left[\frac{\partial \Psi_2(x,y)}{\partial y}\right]_{y=t_{Si}} = -\frac{\varepsilon_{SiGe}}{\varepsilon_{Si}}\left[\frac{\partial \Psi_4(x,y')}{\partial y'}\right]_{y'=t_{SiGe}} \tag{29}$$

5) The potential at source and drain side can be written as

$$\Psi_1(0,0) = V_{bi,s-Si} \tag{30}$$

$$\Psi_2(L,0) = V_{bi,s-Si} + V_{DS} \tag{31}$$

$$\Psi_3(0,0) = V_{bi,SiGe} \tag{32}$$

$$\Psi_4(L,0) = V_{bi,SiGe} + V_{DS} \tag{33}$$

On solving equation (12) to (15) along with the boundary conditions as mentioned in equation (16) to (33) we get the coefficients C_{i1} and C_{i2} which are functions of *x*.

$$C_{11}(x) = \frac{C_{ox}}{\varepsilon_{Si}}\left(\varphi_{s1}(x) - V_{g1}\right) \tag{34}$$

$$C_{12}(x) = -\frac{\left\{\begin{array}{l}\varphi_{s1}(x)\dfrac{\left(C_{ox}C_{Si} + 2C_{Si}C_{SiGe} + 2C_{ox}C_{SiGe}\right)}{C_{Si}} \\ -2V_{sub}C_{SiGe} - \dfrac{(2C_{ox}C_{SiGe} + C_{ox}C_{Si})}{C_{Si}}V_{g1}\end{array}\right\}}{2(C_{SiGe} + C_{Si})t_{Si}^2} \tag{35}$$

$$C_{21}(x) = \frac{C_{ox}}{\varepsilon_{Si}}\left(\varphi_{s2}(x) - V_{g2}\right) \tag{36}$$

$$C_{22}(x) = -\frac{\left\{\begin{array}{l}\varphi_{s2}(x)\dfrac{\left(C_{ox}C_{Si} + 2C_{Si}C_{SiGe} + 2C_{ox}C_{SiGe}\right)}{C_{Si}} \\ -2V_{sub}C_{SiGe} - \dfrac{(2C_{ox}C_{SiGe} + C_{ox}C_{Si})}{C_{Si}}V_{g2}\end{array}\right\}}{2(C_{SiGe} + C_{Si})t_{Si}^2} \tag{37}$$

$$C_{31}(x) = 0 \tag{38}$$

$$C_{32}(x) = -\frac{C_{Si}\left\{2V_{sub} - \dfrac{(2C_{Si} + C_{ox})}{C_{Si}}\varphi_{s1}(x) + \dfrac{C_{ox}}{C_{Si}}V_{g1}\right\}}{2(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{39}$$

$$C_{41}(x) = 0 \tag{40}$$

$$C_{42}(x) = -\frac{C_{Si}\left\{2V_{sub} + \frac{C_{ox}}{C_{Si}}V_{g2} - \frac{(2C_{Si}+C_{ox})}{C_{Si}}\varphi_{s2}(x)\right\}}{2(C_{SiGe}+C_{Si})t_{SiGe}^2} \quad (41)$$

In the above coefficients C_{ox}, C_{Si} and C_{SiGe} are the gate oxide, strained silicon and relaxed silicon germanium layer capacitance per unit area respectively. Also, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$, $C_{Si} = \frac{\varepsilon_{Si}}{t_{Si}}$ and $C_{SiGe} = \frac{\varepsilon_{SiGe}}{t_{SiGe}}$ in which ε_{Si}, ε_{SiGe} and ε_{ox} are the permittivity and t_{Si}, t_{SiGe} and t_{ox} are the s-Si, relaxed $Si_{1-X}Ge_X$ layers and gate oxide thickness respectively.

On solving the 2-D Poisson's equation and the 2-D potential equations as mentioned in equation (12) to (15) using the boundary conditions as mentioned in equation (16) to (33) the value of surface potential was found out as

$$\varphi_{s1}(x) = \frac{\psi_{d1}\sinh(\lambda x) - \psi_{s1}\sinh(\lambda(x-L_1))}{\sinh(\lambda L_1)} - \sigma_1 \quad \text{, for} \quad 0 \le x \le L_1 \quad (42)$$

$$\varphi_{s2}(x) = \frac{\psi_{d2}\sinh(\lambda(x-L_1)) - \psi_{s2}\sinh(\lambda(x-L))}{\sinh(\lambda L_2)} - \sigma_2 \text{, for} \quad L_1 < x \le L \quad (43)$$

In the above expression, ψ_{d1}, $\psi_{d2}, \psi_{s1}, \psi_{s2}, \sigma_1$ and σ_2 are the constants with the characteristic length as λ which are defined below.

$$\psi_{d1} = V_P + \sigma_1 \quad (44)$$

$$\psi_{d2} = V_{bi,s-Si} + V_{ds} + \sigma_2 \quad (45)$$

$$\psi_{s1} = V_{bi,s-Si} + \sigma_1 \quad (46)$$

$$\psi_{s2} = V_P + \sigma_2 \tag{47}$$

$$V_p = \frac{\{\psi_{d2}\cos ech(\lambda L_2) + \psi_{s1}\cos ech(\lambda L_1) - \sigma_1 \coth(\lambda L_1) - \sigma_2 \coth(\lambda L_2)\}}{\coth(\lambda L_1) + \coth(\lambda L_2)} \tag{48}$$

where,

$$\lambda = \sqrt{\frac{\alpha^2 - \beta^2}{2\alpha}} \tag{49}$$

$$\sigma_1 = \frac{\alpha\gamma_1 + \beta\gamma_3}{\alpha^2 - \beta^2} \text{ and } \sigma_2 = \frac{\alpha\gamma_2 + \beta\gamma_4}{\alpha^2 - \beta^2} \tag{50}$$

where,

$$\alpha = \frac{\left(2C_{SiGe}C_{Si} + 2C_{ox}C_{SiGe} + C_{ox}C_{Si}\right)}{C_{Si}\left(C_{SiGe} + C_{Si}\right)t_{Si}^2} \tag{51}$$

$$\beta = \frac{2C_{SiGe}}{\left(C_{SiGe} + C_{Si}\right)t_{Si}^2} \tag{52}$$

$$\gamma_1 = \frac{qN_{a,eff}}{\varepsilon_{Si}} - \frac{C_{ox}(2C_{SiGe} + C_{Si})V_{g1}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{53}$$

$$\gamma_2 = \frac{qN_{a,eff}}{\varepsilon_{Si}} - \frac{C_{ox}(2C_{SiGe} + C_{Si})V_{g2}}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{54}$$

$$\gamma_3 = \frac{qN_{a,eff}}{\varepsilon_{SiGe}} + \frac{C_{ox}C_{SiGe}V_{g1}}{C_{SiGe}(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{55}$$

$$\gamma_4 = \frac{qN_{a,eff}}{\varepsilon_{SiGe}} + \frac{C_{ox}C_{SiGe}V_{g2}}{C_{SiGe}(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{56}$$

The minimum value of surface potential along the x-axis is found using equation (42), which is

$$\varphi_{s1,\min} = 2\sqrt{a_1 b_1} - \sigma_1 \tag{57}$$

where,

$$a_1 = -\frac{1}{2\sinh(\lambda L_1)}\left[\psi_{s1}e^{-\lambda L_1} - \psi_{d1}\right] = u_1 + v_1 V_{gs} \tag{58}$$

$$b_1 = -\frac{1}{2\sinh(\lambda L_1)}\left[-\psi_{s1}e^{\lambda L_1} + \psi_{d1}\right] = u_2 + v_2 V_{gs} \tag{59}$$

The virtual cathode potential $\Psi_{1,\min}(y)$ is obtained by substituting using Eq. (57) into Eq. (14)

$$\Psi_{1,\min}(y) = \varphi_{s1,\min} + C'_{11}y + C'_{12}y^2 \tag{60}$$

$$C'_{11} = \frac{C_{ox}}{\varepsilon_{Si}}\left(\varphi_{s1,\min} - V_{g1}\right) \tag{61}$$

$$C'_{12}{}' = -\frac{\left\{\varphi_{s1,\min}\dfrac{\left(C_{ox}C_{Si} + 2C_{Si}C_{SiGe} + 2C_{ox}C_{SiGe}\right)}{C_{Si}} - 2V_{sub}C_{SiGe} - \dfrac{(2C_{ox}C_{SiGe} + C_{ox}C_{Si})}{C_{Si}}V_{g1}\right\}}{2(C_{SiGe} + C_{Si})t_{Si}^2} \tag{62}$$

Further, Ψ_m, the minimum virtual cathode potential is obtained by solving $\left(\dfrac{\partial\Psi_{1,\min}(y)}{\partial y}\right)_{y=y_m} = 0$ and eventually substituting y_m into Eq.(60)

$$\Psi_m = \varphi_{s1,\min} + C'_{11}y_m + C'_{12}y_m^2 \tag{63}$$

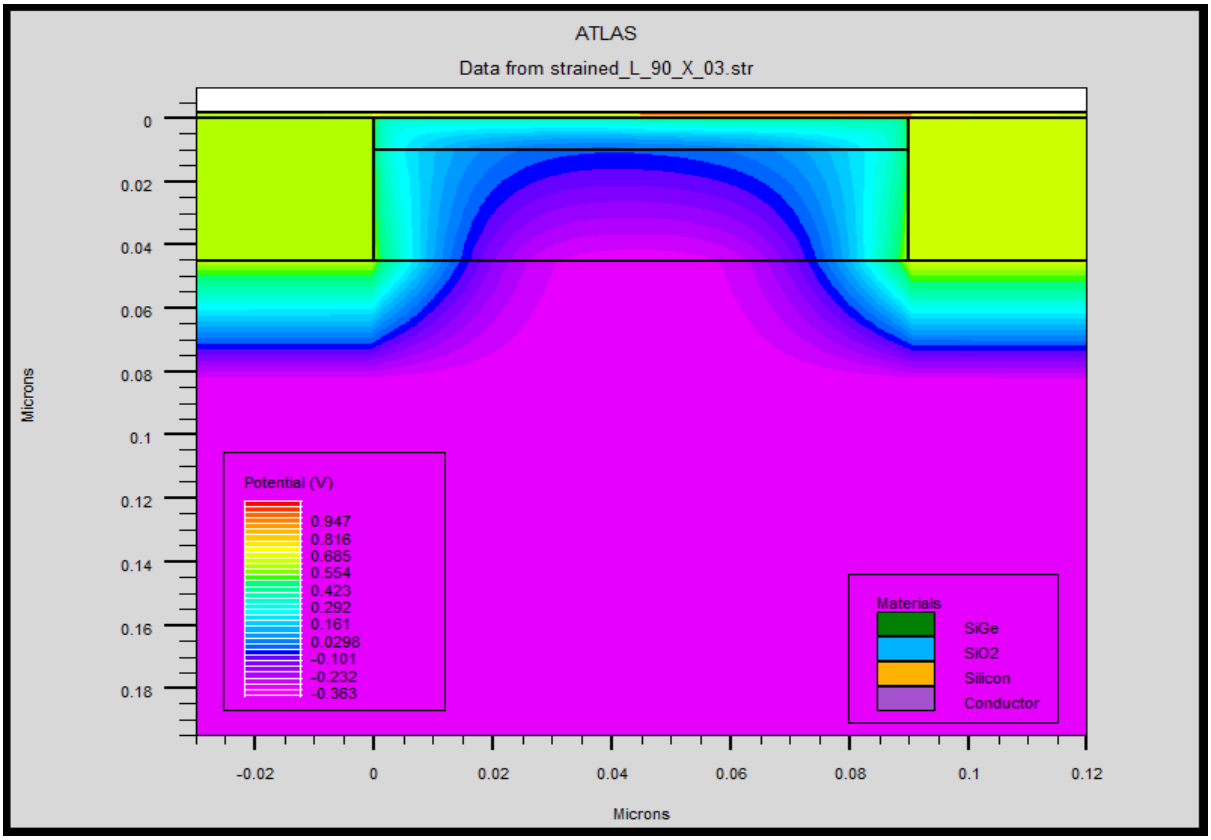

Fig.4.3 2D potential profile of DMG s-Si on SiGe MOSFET extracted from tonyplot with L=90nm.

The variation of 2D potential profile in the structure DMG s-Si on SiGe MOSFET with L=90nm obtained from tonyplot is shown in Fig.4.3. The minimum value of 2D potential is of concern as it is required to obtain the subthreshold current in the device as discussed in the next section.

4.2. Subthreshold Current

Subthreshold current in MOSFET is defined as the current flowing between source and drain terminal when the device is in off state i.e. the gate to source voltage of the device is less than the

threshold voltage. The diffusion current dominates in the subthreshold region of operation and it can be expressed as [18]

$$I_{sub} = \int_0^{t_{Si}} J_n(y)dy \tag{64}$$

where, $J_n(y) = \frac{qD_n n_{\min}(y)}{L_e}\left(1-\exp\left(-\frac{V_{ds}}{V_T}\right)\right)$ (65)

Here, $n_{\min}(y)$, D_n, L_e and V_T are electron concentration at the virtual cathode along the transverse direction, the coefficient of diffusion, effective length and thermal voltage respectively.

$$n_{\min}(y) = \frac{n_i^2}{N_a}\exp\left(\frac{\Psi_{1,\min}(y)}{V_T}\right) \tag{66}$$

In the above equation (66) n_i is the intrinsic carrier concentration. The effective length of the device is considered which is caused due to the source/drain channel depletion region and is expressed as $L_e = L_g - (L_s + L_d) + 2L_D$ where L_g, L_s, L_d and L_D represent the gate length, depletion width due to source, depletion width due to drain & Debye length which can be formulated [19] as

$$L_D = \sqrt{\frac{\varepsilon_{Si}V_T}{qN_a}} \tag{67}$$

$$L_s = \frac{2(V_{bi,Si} - \Psi_m)}{\left(\frac{\partial\Psi}{\partial x}\right)_{x=0}} \tag{68}$$

$$L_d = \frac{2(V_{bi,Si} + V_{ds} - \Psi_m)}{\left(\frac{\partial \Psi}{\partial x}\right)_{x=L}} \tag{69}$$

Here, Ψ_m is the minimum potential point in the channel considering both lateral and transverse direction as mentioned in equation (63).

Now, the subthreshold current could be expressed as

$$I_{sub} = K \int_0^{t_{Si}} \exp\left(\frac{\Psi_{1,\min}(y)}{V_T}\right) dy \tag{70}$$

where, $K = \frac{qD_n V_T n_i^2}{L_e N_a}\left(1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right)$. (71)

The integral of Eq. (70) is solved by dividing the channel thickness into two sections, one from 0 to y_m and other from y_m to t_{Si}, where y_m is the position of minimum virtual cathode potential and the point where field changes its direction. Further, virtual cathode potential is approximated by straight lines in these two regions, similar to the method used in [20], thus, Eq. (70) could be written as

$$I_{sub} = K\left[\int_0^{y_m} \exp\left(\frac{\Psi_{1,\min}(y)}{V_T}\right) dy + \int_{y_m}^{t_{Si}} \exp\left(\frac{\Psi_{1,\min}(y)}{V_T}\right) dy\right] \tag{72}$$

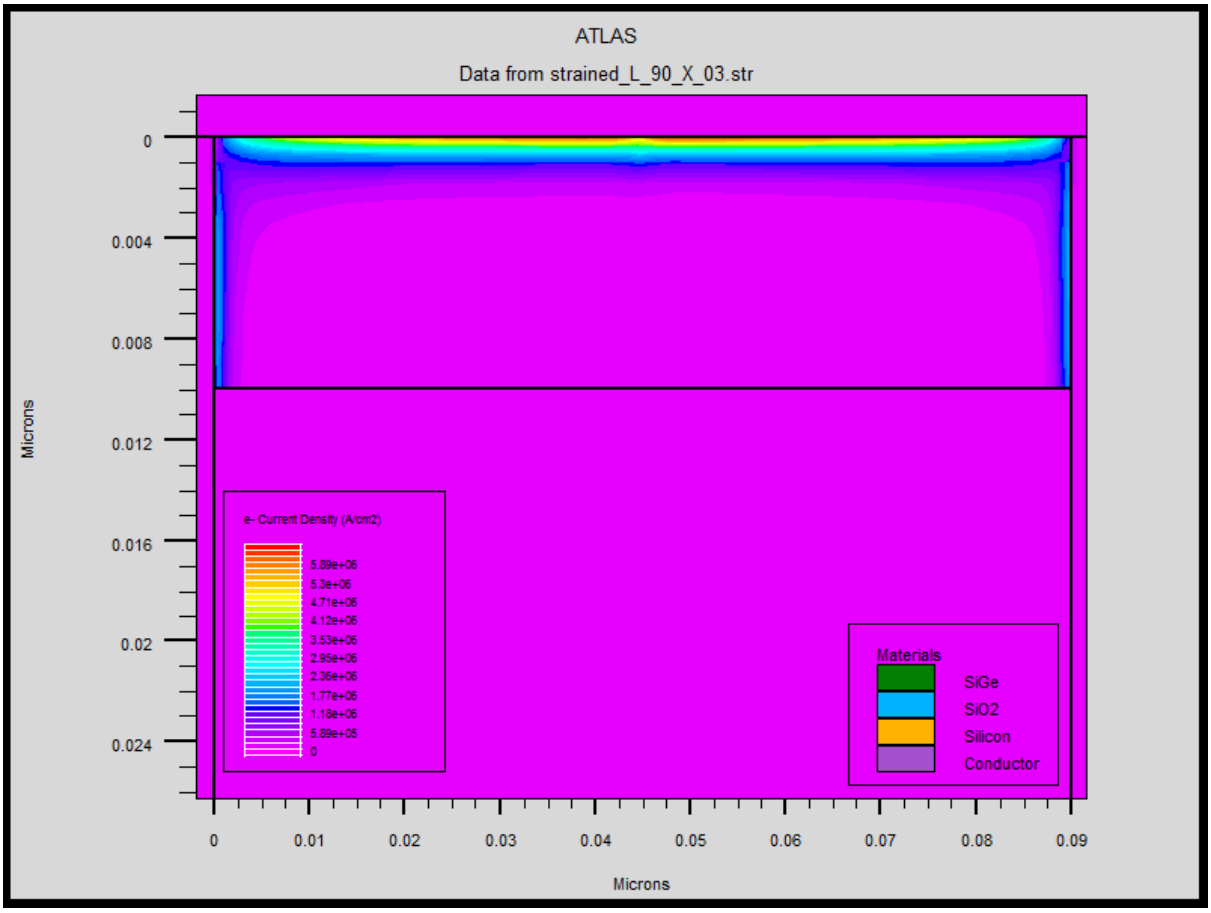

Fig.4.4 e-current density of DMG s-Si on SiGe MOSFET extracted from tonyplot with L=90nm.

The e-current density profile for DMG s-Si on SiGe MOSFET with L=90nm. is shown in Fig.4.4. As the device is of n-type the channel is formed when external voltages are applied in the gate and drain terminals.

Equation (72) could be simplified written in simplified form as follows:

$$I_{sub} = KV_T\left(\frac{I_f}{E_f} + \frac{I_b}{E_b}\right) \tag{73}$$

in which,

$$I_f = \exp\left(\frac{\Psi_{1,\min}(y=0\ )}{V_T}\right) - \exp\left(\frac{\Psi_{1,\min}(y=y_m)}{V_T}\right) \tag{74}$$

$$I_b = \exp\left(\frac{\Psi_{1,\min}(y=y_m\ )}{V_T}\right) - \exp\left(\frac{\Psi_{1,\min}(y=t_{Si})}{V_T}\right) \tag{75}$$

$$E_f = \left(\Psi_{1,\min}(y=0) - \Psi_{1,\min}(y=y_m)\right) / y_m \tag{76}$$

$$E_b = \left(\Psi_{1,\min}(y=y_m) - \Psi_{1,\min}(y=t_{Si})\right) / (t_{Si} - y_m) \tag{77}$$

in which,

$$\Psi_{1,\min}(y=0) = \varphi_{s1,\min} \tag{78}$$

$$\Psi_{1,\min}(y=y_m) = \varphi_{s1,\min} - \left(\frac{C_{11}'^2}{2C_{12}}\right) + \left(\frac{C_{11}'^2}{4C_{12}}\right) \tag{79}$$

$$\Psi_{1,\min}(y=t_{Si}) = \varphi_{s1,\min} + C_{11}' t_{Si} + C_{12}' t_{Si}^2 \tag{80}$$

In fig.4.5 the plot between subthreshold current versus gate-to-source voltage is shown for gate lengths $L = 70,90,110nm$ while keeping other device parameters constant. It is seen that the off state leakage current increases at shorter gate lengths which is quite obvious as the SCEs increases. Since the predicted model is valid only in the subthreshold region of operation because only diffusion phenomenon is considered in the modeling section, therefore the agreement in matching with the simulation results is valid up to the threshold voltage of the device.

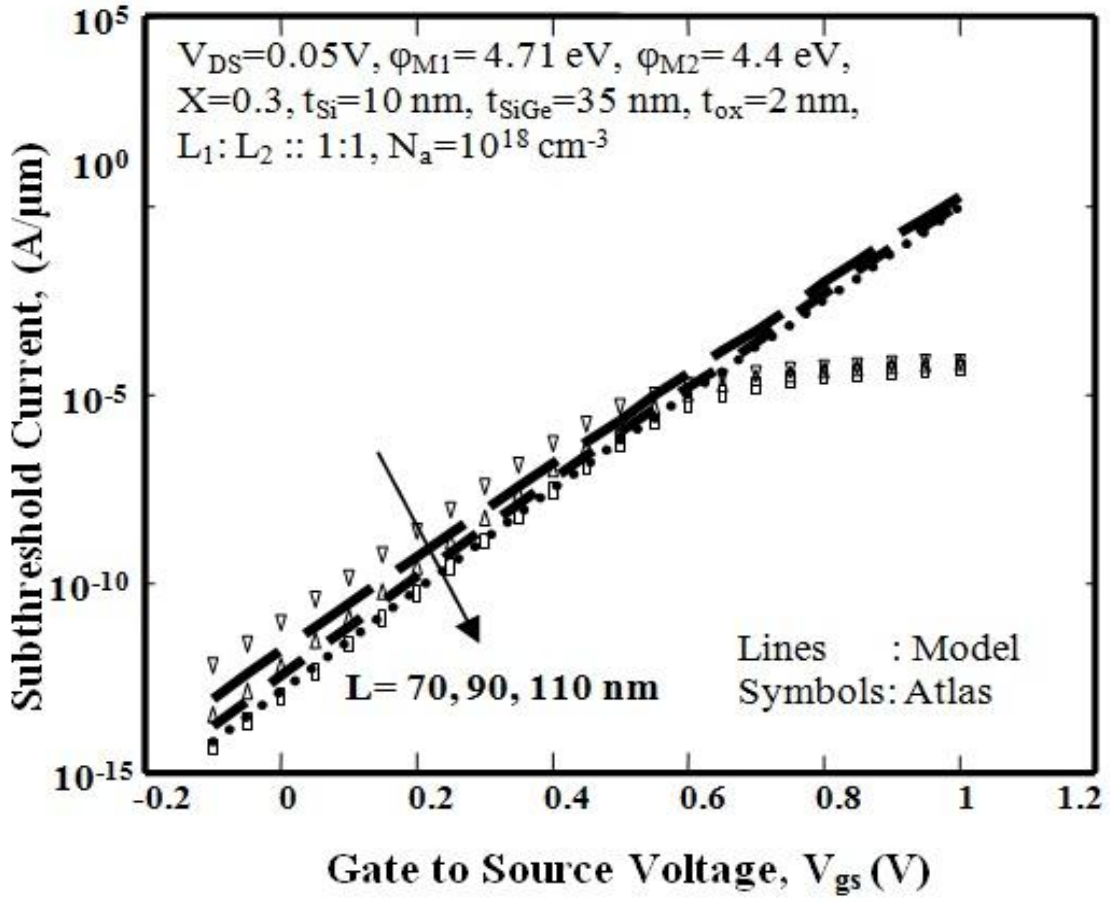

Fig.4.5 Subthreshold current (I_{sub}) vs. V_{GS} for channel length $L = 70,90,110nm$.

The plot of subthreshold current versus gate to source voltage (V_{GS}) is shown in Fig. 4.6 while varying the concentration of Ge in the substrate. As the strain in the channel is directly proportional to the amount of Ge mole fraction content in the substrate due to larger mismatch in lattice constants of Si and SiGe hence the mobility of carriers in the channel get enhanced. Also it is clearly seen that the off current increases at higher strain which is obvious as there is a significant reduction in threshold voltage at higher strain [15].

In Fig. 4.7 the graph between subthreshold current and gate to source voltage is examined while varying work functions of control gate while keeping the work function of screen gate

fixed. The different control gate metal used are 4.6 eV (Mo: Molybdenum), 4.71 eV (Rh: Rhenium), 4.8 eV (Au: Gold) and 4.9 eV (InAs: Indium Arsenide) whereas the screen gate metal is fixed to 4.4 eV (Tungsten). A decrease is leakage current is observed corresponding to an increase in control gate metal work function which may be attributed to the fact that the flat band voltage increases at higher work function. Hence for reducing the subthreshold leakage current in the device a higher control gate metal work function can be chosen.

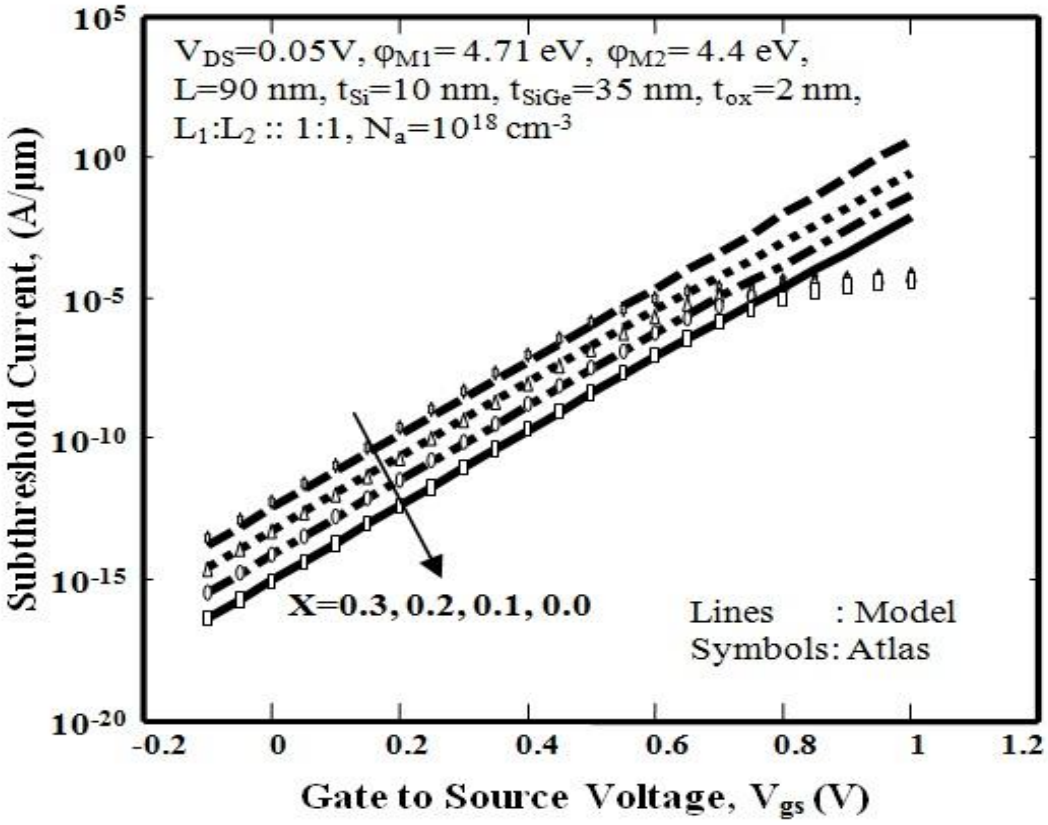

Fig.4.6 Subthreshold current (I_{sub}) vs. V_{GS} for mole fractions $X = 0.3,0.2,0.1,0.0$.

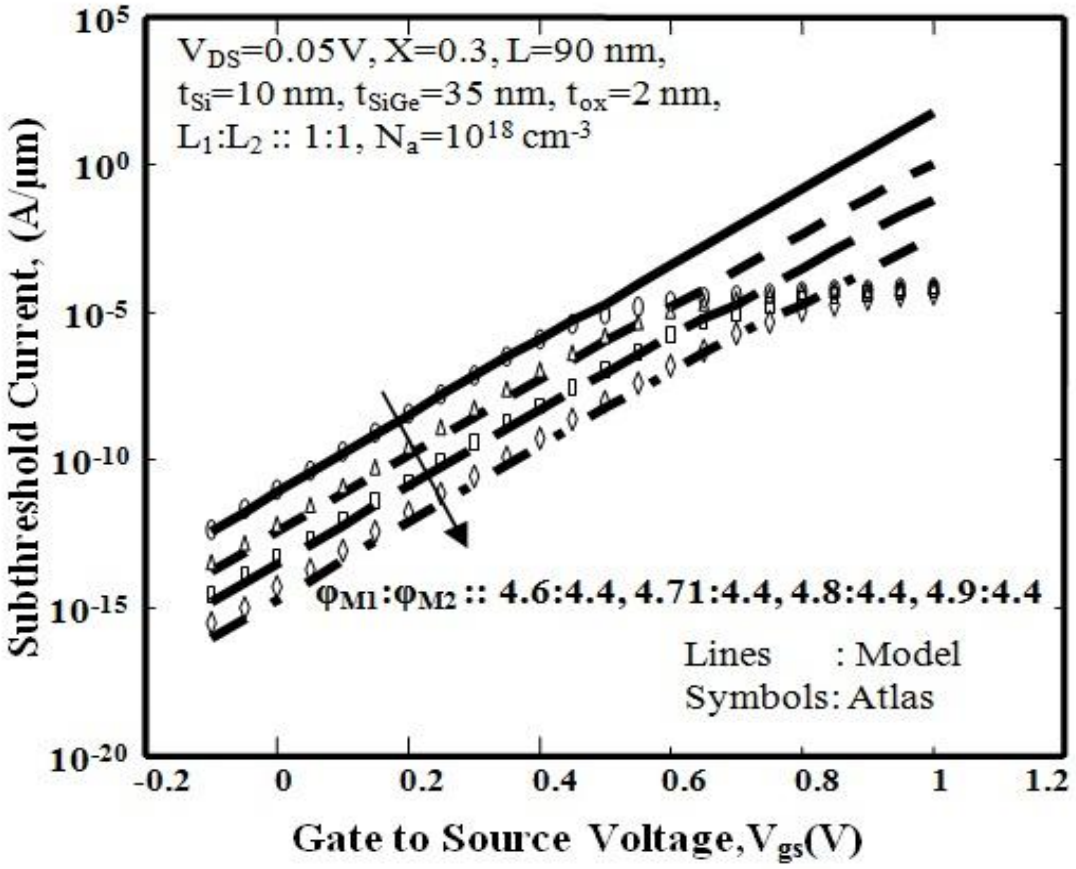

Fig.4.7 Subthreshold current (I_{sub}) vs. V_{GS} for $\varphi_{M1} : \varphi_{M2} :: 4.6 : 4.4$, $4.71 : 4.4, 4.8 : 4.4, 4.9 : 4.4$.

In Fig 4.8 the graph between subthreshold current and gate to source voltage is plotted while varying the control gate to screen gate length ratio with other device parameters fixed as mentioned in the graph. It is observed that the subthreshold leakage current is least for $L_1 : L_2 :: 2 : 1$ followed by $L_1 : L_2 :: 1 : 1$ and $L_1 : L_2 :: 1 : 2$. It is due to the fact that the barrier height between source and channel increases with higher control gate length [21].

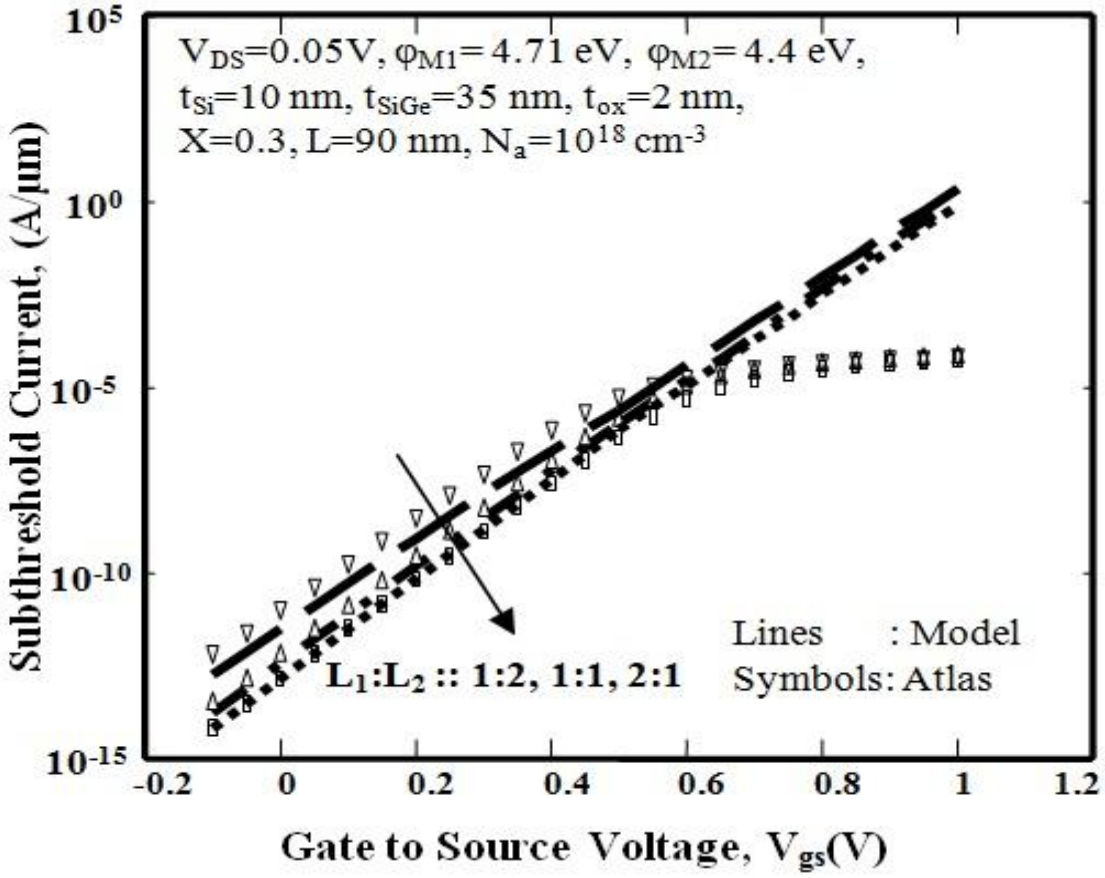

Fig.4.8 Subthreshold current (I_{sub}) vs. V_{GS} for length ratios $L_1 : L_2$ ::1:2,1:1,2:1.

CHAPTER 5

SUBTHRESHOLD SWING FORMULATION

5.1 Subthreshold Swing

Subthreshold swing is another important parameter which helps in determining the switching speed of any device from its off state to on state. It indicates the transition speed between different states of the device. Lower value of subthreshold swing is desirable as the device with lower subthreshold swing works faster. Mathematically, subthreshold swing is defined as the inverse of subthreshold slope which can be expressed as follows:

$$S = \left(\frac{\partial \log I_{sub}}{\partial V_{gs}} \right)^{-1} \tag{81}$$

Further expressing Eq. (81) in terms of potential function as:

$$S = V_T (\ln 10) \times \left(\frac{\partial \varphi_{s1,\min}}{\partial V_{gs}} \right)^{-1} \tag{82}$$

Equation (82) can be further modelled and simplified as follows:

$$S = V_T (\ln 10) \times \left[\frac{a_1 v_2 + b_1 v_1}{\sqrt{a_1 b_1}} + n \right]^{-1} \tag{83}$$

Here a_1 and b_1 are defined in equations (58) and (59). The other coefficients u_1, u_2, v_1 and v_2 are obtained by further solving equations (58) and (59)which are expressed below:

$$u_1 = \frac{V_{P11} + m_1 - (V_{bi,s-Si} + m_1)e^{-\lambda L_1}}{2\sinh(\lambda L_1)} \tag{84}$$

$$u_2 = \frac{(V_{bi,s-Si} + m_1)e^{+\lambda L_1} - (V_{P11} + m_1)}{2\sinh(\lambda L_1)} \tag{85}$$

$$v_1 = \frac{V_{P12} - n(1 - \exp(-\lambda L_1))}{2\sinh(\lambda L_1)} \tag{86}$$

$$v_2 = \frac{n(1 - \exp(\lambda L_1)) - V_{P12}}{2\sinh(\lambda L_1)} \tag{87}$$

$$V_{P11} = \frac{\left\{\begin{array}{l} m_2(\cos ech(\lambda L_2) - \coth(\lambda L_2)) + m_1(\cos ech(\lambda L_1) - \coth(\lambda L_1)) + \\ (V_{bi,s-Si})\cos ech(\lambda L_1) + (V_{bi,s-Si} + V_{ds})\cos ech(\lambda L_2) \end{array}\right\}}{\coth(\lambda L_1) + \coth(\lambda L_2)} \tag{88}$$

$$V_{P12} = \frac{-\{n\ (\cos ech(\lambda L_1) - \coth(\lambda L_1)) + n\ (\cos ech(\lambda L_2) + \coth(\lambda L_1))\}}{\coth(\lambda L_1) + \coth(\lambda L_2)} \tag{89}$$

Here,m_1, m_2 and n are represented as follows:

$$m_1 = \left(\frac{\alpha A_1 + \beta C_1}{\alpha^2 - \beta^2}\right). \tag{90}$$

$$m_2 = \left(\frac{\alpha\ A_2 + \beta C_2}{\alpha^2 - \beta^2}\right). \tag{91}$$

$$n = \left(\frac{\alpha B - \beta D}{\alpha^2 - \beta^2}\right) \tag{92}$$

$$A_1 = \frac{qN_a}{\varepsilon_{Si}} + B(V_{FB1,f})_{sSi} \tag{93}$$

$$A_2 = \frac{qN_a}{\varepsilon_{Si}} + B\left(V_{FB2,f}\right)_{sSi} \tag{94}$$

$$C_1 = \frac{qN_a}{\varepsilon_{SiGe}} - D\left(V_{FB1,f}\right)_{sSi} \tag{95}$$

$$C_2 = \frac{qN_a}{\varepsilon_{SiGe}} - D\left(V_{FB2,f}\right)_{sSi} \tag{96}$$

$$B = \frac{C_{ox}(2C_{SiGe} + C_{Si})}{C_{Si}(C_{SiGe} + C_{Si})t_{Si}^2} \tag{97}$$

$$D = \frac{C_{ox}}{(C_{SiGe} + C_{Si})t_{SiGe}^2} \tag{98}$$

In Fig 5.1 the plot between the subthreshold swing is displayed at different gate lengths of the device while varying the control gate to screen gate length ratio. It is seen that subthreshold swing is less for longer length of control gate, i.e., for $L_1 : L_2 :: 2:1$ the switching characteristics is superior to the other cases. It is so because the subthreshold slope is the highest for the case $L_1 : L_2 :: 2:1$ which can be clearly seen from fig.4.7. Also for the case $L_1 : L_2 :: 1:2$ the subthreshold swing achieves the maximum value since the slope in the subthreshold region is the least.

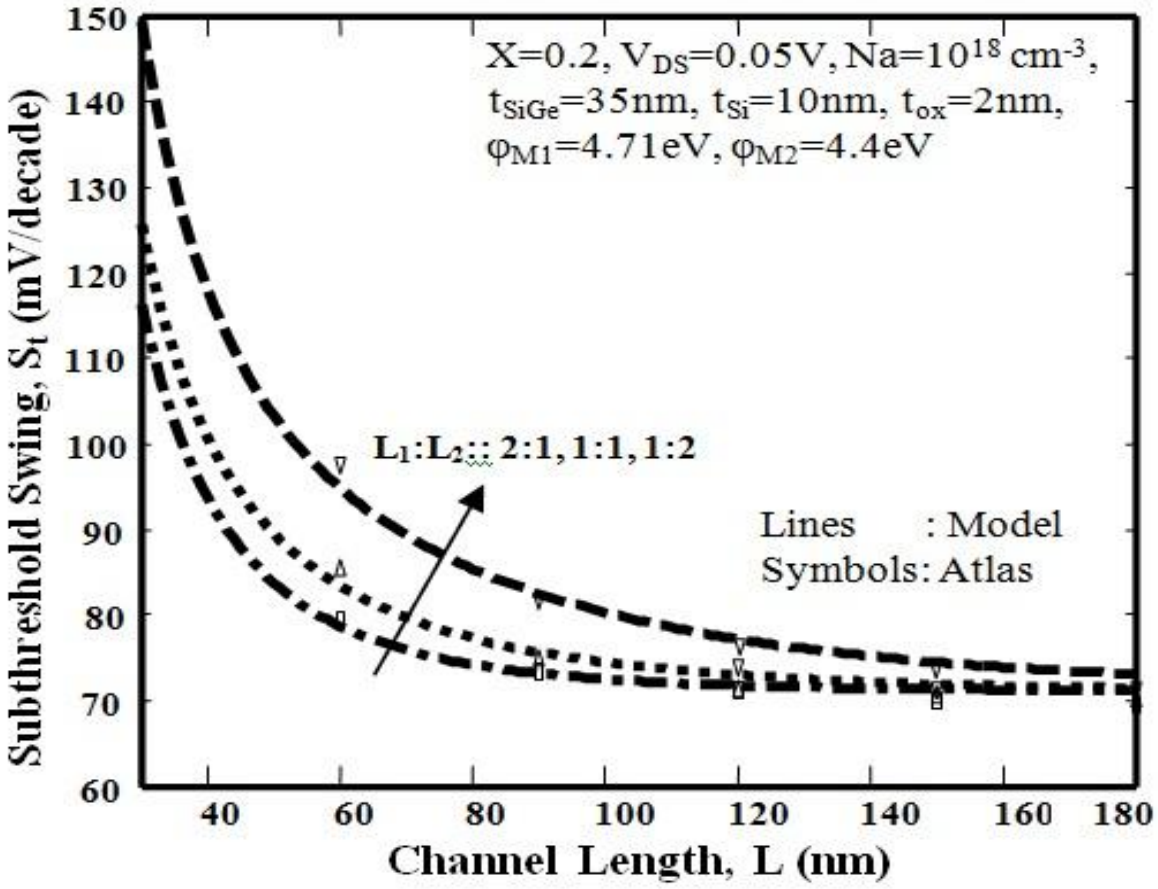

Fig.5.1 Subthreshold swing (S_t) versus channel length (L) for $L_1 : L_2$ ::1:2,1:1,2:1.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The 2-D analytical model for subthreshold current was performed by varying different device parameters such as channel gate length, mole fraction content of germanium, control to screen gate length ratio and different control to screen gate metal work function ratio and a comparison based analysis was done. Further a subthreshold swing model was developed and was calculated for different gate lengths by varying the control to screen gate length ratio. It is observed that for shorter channel lengths the subthreshold leakage current increases. Further, the leakage current also increases with greater strain applied in the channel. By choosing the control gate metal work function of higher work function leakage current can be reduced. Finally it was seen that smaller control to screen gate length ratio causes higher leakage current and also has a greater subthreshold swing.

6.2 Future Work

In future on current modeling, analog and RF performance and effect of temperature on the device can be done.

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